

WHAT IS CLAIMED IS:

1 1. A method of programming a floating gate transistor, the floating
2 gate transistor comprising a source of a first conductivity type, a drain of a second
3 conductivity type, the source and drain formed in a semiconductor region of a third
4 conductivity type and spaced apart by a channel, a floating gate extending over at least a
5 portion of the channel, and a control gate extending over at least a portion of the floating
6 gate, the method comprising the steps of:

7 biasing the control gate of said transistor with a first voltage;

8 biasing the source of said transistor with a second voltage that is less than
9 the first voltage; and

10 applying a programming voltage to the drain of said transistor, the
11 programming voltage being substantially equal to the second voltage to program the
12 floating gate to a logic "1" and being substantially zero to program the floating gate to a
13 logic "0."

1 2. A flash EEPROM memory array comprising:

2 a plurality of memory cells arranged in a matrix of rows and columns, each
3 memory cell including:

4 a portion of a semiconductor substrate of a first conductivity type;

5 a drain region of a second conductivity type formed into said substrate;

6 a source region of said second conductivity type formed in said substrate
7 in spaced alignment with said drain region with a channel region therebetween, said
8 source region having a more abrupt profile grade relative to the surface of said substrate
9 than said drain region;

10 a first gate insulation formed on said major surface of said substrate and
11 having a first thickness;

12 a floating gate electrode formed on said first gate insulation and
13 asymmetrically located over said channel region and having a portion over both drain and
14 source regions wherein a greater portion is over the source region than the drain region;

15 a second gate insulation formed on said floating gate and having a second
16 thickness greater than said first thickness;

a control gate electrode formed on said second gate insulation and overlapping said floating gate electrode, said control gate electrode extending from said cell to adjacent cells in a column;

means connecting said drain regions of said plurality of memory cells in an array of columns;

means connecting said control gate electrodes of said plurality of memory cell in an array of rows, said rows substantially perpendicular to said columns; and

means connecting said source regions to a common source, wherein programming of a cell to a high state is by applying a positive bias to said common source and to said means connecting said control gate electrodes associated with said cell, to inject a charge from the source region into the floating gate through the first gate insulation, and wherein erasing of a cell is by applying a high voltage to the common source when the control gate electrode is grounded and the drain region is floating.

3. In a flash EEPROM array, wherein said array comprises a plurality of memory cells arranged in a matrix of rows and columns, each memory cell including a portion of a semiconductor substrate of a first conductivity type; a drain region of a second conductivity type formed into said substrate; a source region of said second conductivity type formed into said substrate in spaced alignment with said drain region with a channel region therebetween, said source region having a more abrupt profile grade relative to the surface of said substrate than said drain region, a first gate insulation formed on said major surface of said substrate and having a first thickness; a floating gate electrode formed on said first gate insulation and asymmetrically located over said channel region and having a portion over both drain and source regions wherein a greater portion is over the source region; a second gate insulation formed on said floating gate and having a second thickness greater than said first thickness; a control gate electrode formed on said second gate insulation and overlapping said floating gate electrode, said control gate electrode extending from said cell in one direction to adjacent cells in a column; means connecting said drain regions of said plurality of memory cells in an array of columns; means connecting said control gate electrodes of said plurality of memory cell in an array of rows, said rows substantially perpendicular to said columns; and means connecting said source regions to a common source, a method of programming a cell in said EEPROM array comprising:

selecting a cell for programming to a high state or a “low” state, wherein
said cell is associated with one of a plurality of means connecting said control gate
electrodes and one of a plurality of means connecting said drain regions;
applying to said means connecting said source regions a first voltage;
applying to the selected means connecting said control gate a second voltage;
applying to the selected means connecting said drain regions a third
voltage substantially equal to said second voltage if said floating gate transistor is to be
programmed to a “high” state, and grounding said drain if said floating gate transistor is
to be programmed to a “low” state; and
floating all other means not associated with said selected cell.

4. A method of programming a floating gate transistor, said floating
gate transistor comprising a source, a drain spaced apart from said source, said source and
drain being of a first conductivity type and formed in a semiconductor region of a second
conductivity type, a channel extending between said source and drain, a floating gate
extending over at least a portion of said channel, and a control gate extending over at least
a portion of said floating gate, said method comprising the steps of:
applying a first voltage to said gate;
applying a second voltage to said source; and
applying to said drain a third voltage substantially equal to said second
voltage if said floating gate transistor is to be programmed to a “high” state and
grounding said drain if said floating gate transistor is to be programmed to a “low” state.

5. The method of programming a floating gate transistor according to
claim 4, further comprising the steps of:
grading said source greater than said drain;
diffusing said source with impurities to increase its conductivity relative to
said semiconductor region.

6. A flash memory, comprising:
a plurality of floating gate transistors, each transistor having a control gate
a floating gate, a drain and a source, said plurality arranged in an N-row by M-column
array, where N and M are integers greater than or equal to one;
N word lines, each word line connecting together the control gates of
transistors in a common and corresponding row; and

7 M bit lines, each bit line connecting together the drains of transistors in a
8 common and corresponding column,
9 wherein a specific floating gate transistor of the plurality is selected and
10 programmed by applying a first voltage to the control gates of the transistors in the row in
11 which the specific transistor is disposed, applying a second voltage to the source of the
12 specific transistor and grounding the drain of the specific transistor.

1 7. The flash memory of claim 6, wherein the sources of all transistors
2 are connected together as a common source.

1 8. The flash memory of claim 6, wherein the second voltage is greater
2 than ground potential.

1 9. The flash memory of claim 6, wherein the source of each transistor
2 comprises a first doped region having a first conductivity type extending into a
3 semiconductor substrate having a second conductivity type of a charge opposite to the
4 first conductivity type, thereby forming a first p-n junction.

1 10. The flash memory of claim 9, wherein the drain of each transistor
2 comprises a second doped region of the first conductivity type, which is laterally spaced
3 from the first doped region and extends into the substrate, thereby forming a second p-n
4 junction.

1 11. The flash memory of claim 10, wherein the first doped region is a
2 double-diffused region comprising a first sub-region of a first dopant and a second sub-
3 region of a second dopant species, the first and second dopant species being of the first
4 conductivity type.

1 12. The flash memory of claim 11, wherein the first doped region
2 extends deeper into the substrate than the first doped region.

1 13. The flash memory of claim 12, wherein the floating gate of each
2 transistor is disposed vertically above and interposed between an oxide layer and the
3 substrate such that the first doped region horizontally overlaps the floating gate to a
4 greater extent than a horizontal overlap of the second doped region.